

High Voltage Resistant Edge Structure for Semiconductor Components

The invention relates to a high voltage resistant edge structure in the edge region of a semiconductor component according to the preamble of Patent Claim 1.

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Accordingly, a high voltage resistant edge structure in the edge region of a semiconductor component is provided, which has a semiconductor body, at whose first surface at least one inner zone of the first conductivity type is adjacent, at least one floating guard ring arranged in the inner zone, and at least one inter-ring zone of 10 the second conductivity type arranged between the floating guard rings.

In semiconductor elements, particularly in high voltage resistant power semiconductor components, voltage breakthroughs preferably arise in their edge region outside the doping zones, since the electrical field intensity is especially great there due to the 15 curvature of the doping zones which is conditioned by the edge. To avoid such voltage breakthroughs, doping zones are arranged in rings about the semiconductor components. These annular doping zones reduce local field intensity peaks in the edge region of the semiconductor component.

20 Such protective rings are described in the Canadian patent 667,423, for example. But since the field intensity must be reduced to almost zero in each of the guard rings, the floating guard rings described there must be dimensioned very wide toward the edge. This edge structure consumes a great deal of space, accordingly.

25 Furthermore, US 3,405,329 teaches edge structures of semiconductor components with what are known as magnetoresistive rings. These magnetoresistive rings are constructed so as to achieve a largely uniform voltage distribution along the surface of the semiconductor body of a semiconductor component. In this way, field intensity peaks which favor the occurrence of a breakthrough are avoided. The realization of

these magnetoresistive rings in the edge region of the semiconductor component is likewise very costly in terms of space.

US 4,468,686 teaches a high voltage resistant edge structure with magnetoresistive rings and annular doping zones arranged under the magnetoresistive rings. These annular doping zones essentially consist of a plurality of cascaded MOS transistors. The design of this edge structure likewise takes up a large amount of space in the edge region of the semiconductor component.

5 Proceeding on the basis of this prior art, it is the object of the present invention to set forth a simple and space-efficient embodiment of a high voltage resistant edge structure for semiconductor components, which further ensures a breakthrough voltage at a reproducible level.

10 This object is inventively achieved by an edge structure of the species which has the features of the Patent Claim 1.

Accordingly, a species-related edge structure is provided, in which the conductivities and/or geometries of the floating guard rings and/or the inter-ring zones are set such 20 that their charge carriers are totally depleted when blocking voltage is applied.

The inventive edge structure achieves a modulation of the electrical field both at the surface and in the volume of the semiconductor. With appropriate dimensioning of the inventive edge structure, the field strength maximum can be easily shifted into the 25 depth of the semiconductor body; that is, into the region of the vertical p-n junction. Thus, there can always be a suitable design for an edge structure over a wide range of concentrations of p and n doping, which design allows a "soft" leakage of the electrical field in the volume.

In a particularly advantageous embodiment of the present invention, the floating guard rings have the same width, whereby the width of the inter-ring zones arranged between the individual floating guard rings increases in the direction of the edge of the semiconductor component.

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In a further advantageous embodiment, the width of the floating guard rings decreases in the direction of the edge of the semiconductor component, and the inter-ring zones between the individual floating guard rings have the same width, respectively.

10 Beyond this, the depth of the floating guard rings can be varied in the direction of the edge of the semiconductor component. In particular, it is advantageous when the depth of the floating guard rings decreases in the direction of the edge of the semiconductor component.

15 Accordingly, the remaining design parameters for the inventive edge structure include the widths, spacings, and depths of the floating guard rings, which can be defined using lithographic masks. An optimal edge structure can thus be designed for any semiconductor component, and particularly for an arbitrary range of blocking voltages of semiconductor components, using realistically simple means.

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The subsection of the floating guard rings advantageously has a trench-shaped cross-section in the shape of a V or U. The V-shaped or U-shaped form of the cross-section, can be produced easily by an isotropic or anisotropic etching process, respectively, and a subsequent deposition process.

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What is known as a space charge region stopper is also located in the edge region of the semiconductor component. Space charge region stopper refers to an electrode or a heavily doped diffusion zone in the outermost edge region, which defines the lateral extent of the space charge zone beyond the floating guard rings, or respectively,

defines the electrical field. The space charge region stopper usually provides at least a multiple of the breakthrough charge as breakthrough voltage. As space charge region stopper, a heavily doped zone of the same conductivity type as the epitaxial layer can be provided. Depending on the respective requirements, it would also be imaginable

5 to realize the space charge region stopper as what is known as a "damage-implanted" region (implantation zone) or as a metal electrode that is shorted to the substrate material of the semiconductor body, respectively.

The inventive edge structure is expediently provided with at least one magnetoresistor
10 in the direction of the edge, which guarantees the component a good electrostatic protection against mobile parasitic charges in its housing. It has also proven expedient to lead the cathode electrode (in MOSFETs their source electrode), which is situated adjacent the edge structure, up vertically in the direction of the edge region – that is, out of the semiconductor body – in order to allow the electrical field to escape
15 from the semiconductor body.

For the overall edge structure, the corresponding design parameters derive from the maximum permissible electrical field and relate essentially to a boundary surface charge that falls safely below the maximum in the region of the vertically extending
20 p-n junctions. In silicon, this maximum boundary surface charge is approx. 1.5×10^{12} cm⁻². Thus, a given doping profile of the semiconductor body in the edge region results in a layout that is rather simple to manage. The shift of the field strength maximum into the region of the transitions between the individual floating guard rings and inter-ring zones arranged between them is achieved by a net excess of acceptor
25 atoms over the entire surface. This means that, over the whole surface, the sum of the implanted dopants in the floating guard rings must exceed the sum of the doping in the intervening inter-ring zones.

Compared to a conventional edge structure, the inventive edge structure can be dimensioned up to 33% smaller in its lateral extent in the direction of the edge of the semiconductor body.

5 Further advantageous developments of the invention derive from the respective subclaims.

The invention is detailed below with the aid of the exemplifying embodiments indicated in the Figures. Shown are:

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Figure 1 a subsection of a high voltage resistant semiconductor component, which is constructed as a D-MOSFET (or respectively, IGBT) here and which comprises an inventive edge structure;

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Figure 2 a subsection of a further inventive edge structure;

Figure 3 several subsections representing various trench types;

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Figure 4 several exemplifying embodiments representing the creation of a homogenous doping distribution in the edge region of a semiconductor component, which can be purposefully adjusted;

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Figure 5 several subsections representing various edge variations for adjusting a purposeful, "softly" leaking doping concentration in the edge region of a semiconductor component.

To the extent that they are not referenced otherwise, elements that are the same or that have the same function are provided with the same reference characters in all Figures of the drawing.

Figure 1 shows a subsection of a high voltage resistant (power) semiconductor component comprising an inventive edge structure.

The semiconductor component comprises a cell field ZF consisting of a plurality of
5 individual components, which are connected in parallel and are arranged in individual cells Z1...Z3, of which the outermost three cells Z1...Z3 are represented as cutouts only. The cell field ZF is terminated by an edge structure that is provided in the edge region RB of the semiconductor component. The edge region RB refers to the region of the semiconductor component located outside its active cells Z1...Z3 of the cell
10 field ZF.

In Figure 1, the semiconductor body of the semiconductor component is referenced 1. The semiconductor body 1, which consists of silicon substrate, for example, comprises an n-doped inner zone 2 in this embodiment, which is situated adjacent the
15 first surface 3 of the semiconductor body 1 at the source side. The inner zone 2 is typically deposited onto the semiconductor body 1 by an epitaxy process. Particularly in high voltage resistant power semiconductor components having a very high blocking voltage, this epitaxy layer is created with the aid of several consecutive epitaxy steps, wherein a respective epitaxial sublayer is deposited on top of the layer
20 below it. This technique is known as the build-up technique.

At the drain side, a drain zone 4 is adjacent the inner zone 2. If the semiconductor component is constructed as a MOSFET, then the drain zone 4 is typically heavily n-doped. But if the semiconductor component is an IGBT, then the drain zone 4 is also
25 designated as an anode zone and is typically heavily p-doped (represented by brackets in Figure 1). In this case, the boundary surface 5 characterizes the p-n junction between the drain zone 4 and the inner zone 2. Beyond this, the drain zone 4 is adjacent the second surface 6 of the semiconductor body 1 and is connected here surface-wide to the drain electrode 7 and thus to the drain terminal D.

At the source-side surface 3, a plurality of base zones 8 are embedded in the inner zone 2. The base zones 8 comprise the opposite conductivity type to the inner zone 2; that is, they are p-doped in the present case. In the present exemplifying embodiment, at least one heavily n-doped source zone 9 is embedded in each of the base zones 8, 5 respectively. In the present exemplifying embodiment, the base zones 8 and the source zones 9 embedded in them have a trough shape and can be created by ion implantation and/or by diffusion, for example.

The base zones 8 and/or the source zones 9 typically, though not necessarily, have the 10 same cell design as the corresponding cells Z1...Z3 in which they are embedded. Such a cell design can consist of cells in the shape of strips, hexagons, triangles, quadrilaterals, circles, ovals, or some such.

The semiconductor component in Figure 1 is constructed as a vertical D MOSFET (or 15 IGBT, respectively). Of course, the source zones 9 or the base zones 8, respectively, can also be arranged in what is known as a trench. The corresponding semiconductor component would then be a trench MOSFET or a trench IGBT, respectively. It would also be imaginable to give the source zones 9 or the base zones 8 a V-shaped or trapezoidal cross-section, respectively.

20 In Figure 1, the source zones 9 and the base zones 8 are connected in known fashion to the source electrode 10, and thus to the source terminal S, via contact holes 10'. This shunting of the base zone 8 and the source zone 9 makes it possible to keep a parasitic bipolar transistor from being turned on there.

25 Beyond this, a gate electrode 11 that is insulated from the semiconductor body 1 via a thin gate oxide 12 is provided at the first surface 3. The gate electrode 11 is connected to the gate terminal G and can consist of heavily doped polysilicon or

metal, respectively. A field oxide 13 is further provided, which insulates the source electrode 10 from the gate electrode 11 and from the semiconductor body 1.

Finally, the semiconductor component according to Figure 1 has a space charge zone stopper 14. This space charge zone stopper 14 is arranged at the outermost edge region RB of the semiconductor component; that is, directly before its arris. In the present exemplifying embodiment, the space charge zone stopper 14 is constructed in known fashion as a single-stage metal electrode 14' that rises in the direction of the cell field ZF, which is contacted to a heavily n-doped diffusion zone 14''. The metal electrode 14' can also be constructed as a polysilicon electrode, or can be omitted, depending on the application.

Typically, stepped magnetoresistive rings 17 are provided in the edge region Rb of a power semiconductor. Such magnetoresistors 17 are typically single-step or multi-step, these magnetoresistors 17 leading away from the first surface 3 in the direction of the edge. In the exemplifying embodiment according to Figure 1, only one single-step magnetoresistor 17 is shown.

For reasons of optimizing surface area, it has proven advantageous that the gate electrodes 11 of the respectively outermost cells Z1 of the active cell field ZF simultaneously take over the function of the magnetoresistor 17. It has also proven advantageous that the source electrode 10 adjacent the edge structure is likewise led up vertically in the direction of the edge; that is, is led up from the first surface 3 of the semiconductor body 1. This allows the electrical field to escape from the semiconductor body 1.

Guard rings 15 are inventively provided in the edge region RB; that is, outside the active cell field ZF. These guard rings 15, which are lightly p-doped in this exemplifying embodiment, are "floating"; that is, they have an undefined potential. In

the subsection in Figure 1, these floating guard rings 15 are columnar and extend from the first surface 3 of the semiconductor body 1 to deep in the inner zone 2. In the exemplifying embodiment according to Figure 1, four of these floating guard rings 15 are provided.

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The floating guard rings 15 are spaced apart from one another, and the region between the floating guard rings 15 defines an inter-ring zone 16. This inter-ring zone 16 typically, though not necessarily, has the same dopant concentration as the sub-base doping; that is, as the inner zone 2. The lateral and horizontal dimensions and 10 geometries of the floating guard rings 15 and inter-ring zones 16 and their dopant concentration are not discussed further here. These points are described later with the aid of Figures 3 to 5.

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The inter-ring zones 16 are typically produced by what is known as the trench technique. In the present exemplifying embodiment, the trenches of the inter-ring zones 16 extend from the first surface 3 of the semiconductor body 1 deep into the inner zone 2. Of course, it would also be possible for these trenches 16 to extend through the entire inner zone 2 and to connect to the drain zone 4. In principle, it is also conceivable for the trenches 16 to penetrate from the first surface 3 to the second 20 surface 6 at the back of the wafer of the semiconductor body. This situation is described later with the aid of Figure 5.

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Figure 2 illustrates another exemplifying embodiment of an inventive edge structure with reference to a subsection.

In Figure 2, the inter-ring zones 16 are additionally tapered in the direction of the first surface 3 of the semiconductor body. Furthermore, it is particularly advantageous when the source electrode 10 encompasses the corresponding gate electrode 121 in the direction of the edge region RB. That is, the source electrode 10 projects in the

direction of the edge region RB beyond the corresponding outermost gate electrode 11, or respectively, the magnetoresistor 17, and is then taken down again in the direction of the first surface 3 of the semiconductor body 1.

5 The result of this is a structure in the edge structure RB wherein the outermost gate electrode 11, or respectively, magnetoresistor 17, is approximately located in a Faraday cage and thus in a nearly field-free space. Compared to the conventional edge structure that is described in Figure 1, wherein the source electrode 10 is merely drawn up to ever thicker oxide layers of the field oxide 13 in the direction of the edge, 10 the source electrode 10 that encompasses the gate electrode 11 achieves a significant reduction of the electrical field that is directed to the corresponding gate electrode 11.

By virtue of the above described tapering of the annular inter-ring zones 16 to the first surface 3, the electrical field intensity at the end of the metallization of the source 15 electrode 10 can be reduced to below the respective field intensity of the volume. In a complete reversal of the previous design, the metal electrode 14' of the space charge zone stopper 14 in the outermost region of the edge structure can thus be additionally drawn up onto at least one second oxide step of the field oxide 13. In this way, the 20 electrical field distribution in the open area OB of the edge structure – that is, in the region btwen [sic] the space charge zone stopper 14 and the magnetoresistor 17 – is so modified that the field lines of the electrical field can emerge from the semiconductor body 1 at the first surface 3 via the entire open area OB nearly unchanged by the 25 respective electrodes 14', 17. In this way, the diffusion zone 14" under the metal electrode 14' an be significantly reduced in the direction of the gate electrode 11 and of cell field ZF. The width of the above cited open area OB between the space charge zone stopper 14 and the outermost cell Z1 of the cell field ZF can thus be significantly reduced, which leads to a considerable reduction of the surface-area of the inventive edge structure and thus of the corresponding semiconductor component.

In Figure 3, several trechn [sic] types are shown in subsection.

To create the inter-ring zones 16 with the aid of the trechn [sic] technique, trenches 18 are etched into the inner zone 2 of the semiconductor body 1. In Figure 1 and Figure 5 3(a), these trenches 18 are constructed in an ideally columnar fashion. The present exemplifying embodiment, the trenches 18 have a bottom 19 that runs approximately parallel to the first surface 3, and walls 20 that are ideally arranged at a right angle to the first surface 3. Typically, however, these walls 20 are angled at a flank angle α relative to the horizontal, forming a trench 18 with an approximately trapezoidal 10 cross-section which tapers into the depth of the semiconductor body 1 (Figure 3(b)). But this is not absolutely necessary. It would also be conceivable for the trenches 18 to have a cross-section in the form of trenches that are shaped like a V (Figure 3(c)) or a U (Figure 3(d)) in subsection.

15 A few preferred methods for producing a homogenous doping distribution that can be purposefully adjusted in the edge region of a semiconductor component, and thus for producing an inventive edge structure, are described below with the aid of Figure 4. In all subfigures 4(a)-(d) only one individual trench 18 is represented, for the sake of providing a better overview.

20 Trenches 18 in the form of points, strips, or grids are etched into a relatively heavily doped base material of a first conductivity type, for instance into the inner zone 2 (Figure 4(a)). The trenches 18 are epitaxially filled with material of the second conductivity type. Here, the overall charge is set such that a net doping over the 25 whole surface area is approximately zero, and the surface charge does not exceed the breakthrough charge in any spatial direction. A net doping of close to zero means that the number of acceptors (holes) and the number of donators (electrons) in the lateral projection are approximately in balance.

In another embodiment of the present invention, trenches 18 in the form of strips, points, or grids are etched into a lightly doped or undoped base material (Figure 4(b)). Next, the trenches 18 are covered with epitaxially deposited silicon, polycrystalline silicon or boric phosphorous silicate glass with a doping of the first conductivity type.

5 The doping is driven into the surrounding base material; for instance, by a thermal process. The coating is subsequently etched away again. Next, the trenches 18 are filled again with an epitaxially deposited silicon of the second conductivity type.

In an advantageous development, it is also possible to drive the doping of the second
10 conductivity type into the surrounding base material via a coating and a subsequent thermal step (Figure 4(c)). In this case, to achieve a definite separation of the two conductivity zones, dopants with sharply differing diffusion coefficients should be used. The advantage of this procedure is that, given the failure of a trench 18, for instance, due to a particle during the lithography process, the semiconductor
15 component remains fully functional. In the first method cited, on the other hand, this can give rise to a breakdown of the blocking voltage in this region, and thus to the failure of the whole semiconductor component.

Instead of filling the trenches 18 with epitaxially deposited silicon, a hollow space 23
20 can remain in the trenches, as long as the walls 20 are covered by a passivation layer 21 and the hollow space 2, 3 is occluded on top by a lid 22, for instance consisting of boric phosphorous silicate glass (BPSG) (Figure 4(d)).

Figure 5 shows several subsections, with the aid of which different variants of the
25 edge for setting a purposeful, "softly" leaking doping concentration in the edge region of a semiconductor component are represented. In Figure 5, for the sake of a better overview, the structures corresponding to the Figures 1 and 2 were represented only schematically, since what is essential here is the geometry, the dimensions and the

spacings of the trenches 18, particularly in the edge region RB of the semiconductor component.

The trenches 18 can be etched proceeding from the first surface 3, ideally in a self-aligning manner with respect to the actual component processing (for instance, aligned to the polysilicon edge), or proceeding from the back, or respectively, the second surface 6, after the semiconductor body 1 has been ground thin. Anisotropic etching or isotropic etching can be used. In principle, the trenches 18 may also penetrate from the first surface 3 to the back, or respectively, the second surface 6 (Figure 5(a)). If these trenches 18 are doped sufficiently heavily, the relatively expensive epitaxy wafers can be forgone.

By varying the depth of the trenches 18 in the direction of the edge (Figure 5(a) and (c)), it is possible to favorably influence the field intensity distribution in the edge region RB . In Figure 5(c), the depth $t_1 > t_2 > t_3$ of the trenches 18 diminishes continuously in the direction of the edge. In the cell field ZF of the component, the location of the voltage breakthrough can thus be specified.

It would also be imaginable to vary the dopant coating of the trenches in the radial or vertical direction (Figure 5(b)). For example, if trenches 18 with a V-shaped cross-section and an epitaxial filling of these trenches 18 are used, then the shape of the trenches 18 can intentionally use for vertical variation of the implanted charge proportion [sic]. In particular, the flank angle α of the trench walls can also increase in the direction of the edge.

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To achieve an optimally gradual transition of the doping from nearly fully compensated to significantly n or p doped, it is possible either to enlarge the grid, or respectively, the spacings ($d_1 > d_2 > d_3 > d_4$) of two neighboring trenches 18, in the

direction of the edge in a gradual manner (Figure 5(d)), or to reduce the diameter ($r_1 > r_2 > r_3 > r_4 > R_5$) of the trenches 18 in the direction of the edge (Figure 5(e)).

Compared to the initially cited build-up technique, the trench technique, as it is referred to, using etched trenches 18 has the advantage that smaller cell grids can be provided. These smaller cell grids can then comprise a heavier doping, thereby reducing the surface make resistance $R_{DS,ON}$ significantly.

By way of conclusion, it should be expressly stated that it is of course possible to apply any of the structures described in the Figures 3 to 5 alone or, rather advantageously, in combination with one another, in order to achieve the desired doping profile, or respectively, the desired surfacewide doping distribution, in the edge region RB.

Reference Characters

| | | |
|----|----------|--|
| | 1 | semiconductor body |
| | 2 | inner zone |
| 5 | 3 | first surface |
| | 4 | drain zone |
| | 5 | boundary surface, p-n junction |
| | 6 | second surface |
| | 7 | drain electrode |
| 10 | 8 | base zone |
| | 9 | source zone |
| | 10 | source electrode |
| | 10' | contact hole for the source electrode |
| | 11 | gate electrode |
| 15 | 12 | gate oxide |
| | 13 | field oxide |
| | 14 | space charge zone stopper |
| | 14' | metal electrode of the space charge zone stopper |
| | 14" | diffusion region of the space charge zone stopper |
| 20 | 15 | (floating) guard rings |
| | 16 | inter-ring zones |
| | 17 | magnetoresistor |
| | 18 | trenches |
| | 19 | bottom of trenches |
| 25 | 20 | wall of trench |
| | 21 | passivation layer in the trench |
| | 22 | trench lid |
| | 23 | hollow space |
| 30 | α | flank angle of the trench wall |
| | d1...d4 | spacing between two adjacent trenches, trench grid |
| | r1...r5 | trench diameter |
| | t1...t3 | trench depth |
| 35 | OB | open area in the edge region |
| | RB | edge region |
| | Z1...Z3 | cells |
| | ZF | cell field |
| 40 | D | drain terminal |
| | G | gate terminal |
| | S | source terminal |